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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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WELLS ST JOHN ROBERTS GREGORY AND MATKIN
SUITE 1300
601 W FIRST AVENUE
SPOKANE WA 99201-3828

EXAMINER

TRINH, M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 06/20/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/059,644	PAN, PAI-HUNG	
	Examiner	Art Unit	
	Michael M. Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) Responsive to communication(s) filed on 4/18/00 & 5/9/00.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 41-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 41-52 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - a) All
 - b) Some *
 - c) None of the CERTIFIED copies of the priority documents have been:
 1. received.
 2. received in Application No. (Series Code / Serial Number) _____ .
 3. received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

- 15) Notice of References Cited (PTO-892)
- 16) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11 & 12.
- 18) Interview Summary (PTO-413) Paper No(s). 10 .
- 19) Notice of Informal Patent Application (PTO-152)
- 20) Other: _____

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DETAILED ACTION

*** This is a continuation prosecution application (CPA), in which IDS filed April 18, 2000 has been entered as paper number 11, and in which IDS filed May 09, 2000 has been entered as paper number 12. Pending claims 41-52 are remained unchanging by this CPA request. Claims 1-40 were previously canceled.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action. The indicated allowability of claims 41-52 is withdrawn in view of the submitted reference to Kurimoto (5,306,655). Rejections based on the cited reference follow.

Claim Rejections - 35 USC § 102

1. Claims 41,42,45,46,50 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurimoto (5,306,655).

Kurimoto teaches a method (at Figs 13a-13h; col 13, line 21 through col 16) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate 5f formed on a gate oxide dielectric layer 2 formed on a semiconductor substrate (figs 13a; col 13, lines 30+); forming barrier sidewall nitride spacers 10 over sidewalls of the gate and joining the dielectric oxide layer 2 by anisotropically etching a silicon nitride layer 10 (figs 13C-13D); and then oxidizing the substrate to channel oxidants through the gate dielectric layer 2 and underneath the spacers joined therewith and which is outwardly exposed laterally proximate the sidewall spacers, wherein only a portion of the gate 5f at the interface with the gate dielectric oxide layer 2 is oxidized (Fig 13f) while preventing oxidation of the upper parts of side faces of the gate 5f by the action of the barrier insulating nitride spacers 10 (col 13, lines 59-68).

Claim Rejections - 35 USC § 103

2. Claims 43,47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurimoto (5,306,655) taken with Pintchovski et al (5,126,283).

Kurimoto teaches a method for forming a conductive gate of a metal oxide transistor as applied above to claims 41,42,45,46,50, but lack to form a gate having a polysilicon, a conductive reaction barrier layer, and an overlying metal (re claims 43,47).

However, Pintchovski et al teach (at figs 3a-3c; col 5, line 60 through col 6, line 45) to alternatively form a gate having a polysilicon layer 38, a conductive reaction barrier layer 40, and an overlying metal 42.

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to form a multi-layered transistor gate as taught by Pintchovski et al because of the desirability to fabricate high speed devices due to high conductivity of the gate, wherein the conductive reaction barrier layer also acts as a diffusion barrier.

3. Claims 44,48,49,51,52 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kurimoto (5,306,655) taken with Pintchovski et al (5,126,283), as applied to claims 41-43,45-47,50 above, and further of Brigham et al (5,714,413) and Kumagai et al (5,430,313).

Kurimoto already teach to form single sidewall barrier spacers 10 over sidewalls of the gate (Fig 13), which teaching is similar to a first embodiment of the present invention as shown in figure 3, in which single sidewall barrier spacers 34 are used.

The further main difference between the references applied above and the instant claim(s) is as follows: instead of using single sidewall spacers (first embodiment, fig 3 of present application), the present application, in a second embodiment (fig 5) and a third embodiment (fig 7), alternatively teaches to use double sidewall spacers by etching first and second material layers.

However, Brigham et al teach (at figs 2b-2c,3c; col 6, line 60 through col 7, line 6; cols 4-6) to form double sidewall spacers by depositing a second material layer on a first material layer and anisotropically etching the first and second layers to form double sidewall spacers, wherein Brigham expressly teaches “three or more layers of dielectric...are implemented to form a multi-layered spacer structures” (col 6, lines 1-6), and wherein silicon nitride is disclosed.

Kumagai et al teach (at figs 4B-4D; col 3, line 65 through col 4, line 15) to form single sidewall nitride spacers 16 on sidewalls of a gate 14, and alternatively, forming double sidewall nitride spacers including first sidewall nitride spacers 16 and second sidewall nitride spacers 30 by anisotropically etching a deposited first material barrier layer and then anisotropically etching a second deposited material barrier layer (figs 7A-7D; col 5, line 45 through col 6).

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The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, and Kurimoto. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.
Oasc



Michael Trinh
Primary Examiner